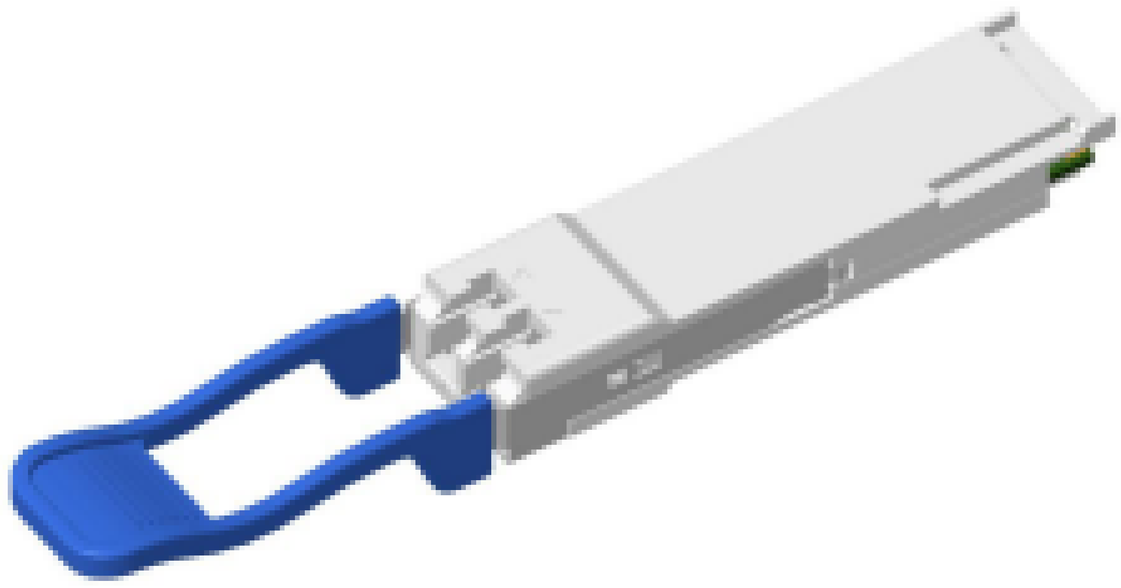
QSFP-LR4-10-40_PSM

40G QSFP+ PSM4 10km Transceivers



FEATURES

- MPO-12 optical interface
- Maximum link length up to 10km
- Up to 10.3125Gb/s data links per lane
- +3.3 V power supply
- QSFP MSA compliant package
- Hot Pluggable
- High performance singal mode DML transmitter
- High sensitivity PIN/TIA optical receiver
- Single Mode operation
- Case Operating temperature : 0 to 70°C
- Data and Control Interfaces
- Tx Data CML/AC Coupled
- Rx Data CML/AC Coupled
- ModSelL LVTTL
- ResetL LVTTL
- ModPrsL LVTTL
- LPMode LVTTL
- 2-wire I2C communication bus
- RoHS 6 compliancE

APPLICATIONS

- 40G BASE Ethernet
- Infiniband EDR interconnects
- Enterprise network

Ordering Information

Part Number	Case Operationg Temperature
QSFP-LR4-10-40_PSM	0~70°C

Description

The QSFP-LR4-10-40_PSM QSFP+ PSM4 optical transceiver is intended for up to 10km reach service with four-lane 10.3125G data rate. It is based on 3.3V DC power supply and operates in the Commercial temperature range. It is compliant with QSFP MSA、SFF-8436 and IEEE802.3ba-2018. Digital diagnostic functions are available via I2C interface， and the control functions can be achieved by LVTTL interfaces on the host， mainly including Module Select(ModSelL)、Module Reset(ResetL)、Low Power Mode(LPMode). The transceiver incorporates a four-laser array which is usually DFB 、 four-PIN diode array 、an integrated four drivers and TIAs IC separately. The differential AC coupled Tx and Rx data interfaces are CML compatible.

Absolute Maximum Parameters

Absolute Maximum Ratings (EXCEEDING THESE RATINGS MAY CAUSE IRREVERSIBLE DAMAGE TO THE DEVICE)					
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Storage Temperature	T_{stg}	-40	+95	ºC	Exceeding the absolute maximum ratings may cause irreversible damage to the device. The device is not intended to be operated under the condition of simultaneous absolute maximum rat- ings, which may cause irreversible damage to the device.
Case Operating Temperature (Commercial)	T_O	0	70	ºC	
Relative Humidity - Storage	R_{HS}	0	95	%	
Relative Humidity - Operating	R_{HO}	0	85	%	
Supply Voltage	VCC	-0.3	3.6	V	

Operating conditions

Recommended Operating Conditions						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Case Operating Temperature	T_{case}	0	-	+70	ºC	
DC Supply Voltage	VCC	3.135	-	3.465	V	
Module Supply Current	I_{in}	-	-	1060	mA	

Electrical Characteristics

Transmitter Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Differential Data input Swing	V_{in}	180	-	900	mV	
Tx Differential Input Impendence	Z_{in}	90	100	110	Ω	
Tx Differential Output Impendence	Z_{out}	45	50	55	Ω	
ResetL Disable Voltage	V_r	2.0	-	Vcc+0.3	V	
ResetL Enable Voltage	V_{rEN}	0	-	0.8	V	
ModSelL Disable Voltage	V_m	2.0	-	Vcc+0.3	V	
ModSelL Enable Voltage	V_{mEN}	0	-	0.8	V	
Receiver Electrical Characteristics						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Differential Data Output Swing	V_{out}	180	-	900	mV	
Rx Differential Output Impendence	Z_{out}	90	100	110	Ω	
IntL Assert Voltage	V_{Int}	VCC-0.5	-	VCC+0.3	V	
IntL De-assert Voltage	VD_{Int}	0	-	+0.4	V	

Optical Specification

Transmitter Optical Specification						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Signal Rate|Each Lane			10.3125 ±100ppm		Gbps	
Lane Wavelength	L0	1295	1310	1325	nm	
	L1	1295	1310	1325	nm	
	L2	1295	1310	1325	nm	
	L3	1295	1310	1325	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power|Each Lane	P_{avg}	-7		2.5	dBm	
Optical Modulation Amplitude|Each Lane	OMA			2.5	dBm	1
Transmitter and dispersion penalty|Each Lane	TDP			2.6	dB	
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Average launch power of OFF transmitter|Each Lane				-30	dBm	
Extinction Ratio	ER	3.5			dB	
Spectral Width|20dB				1	nm	
Transmitter Reflectance				-12	dB	
Optical return loss tolerance				20	dB	

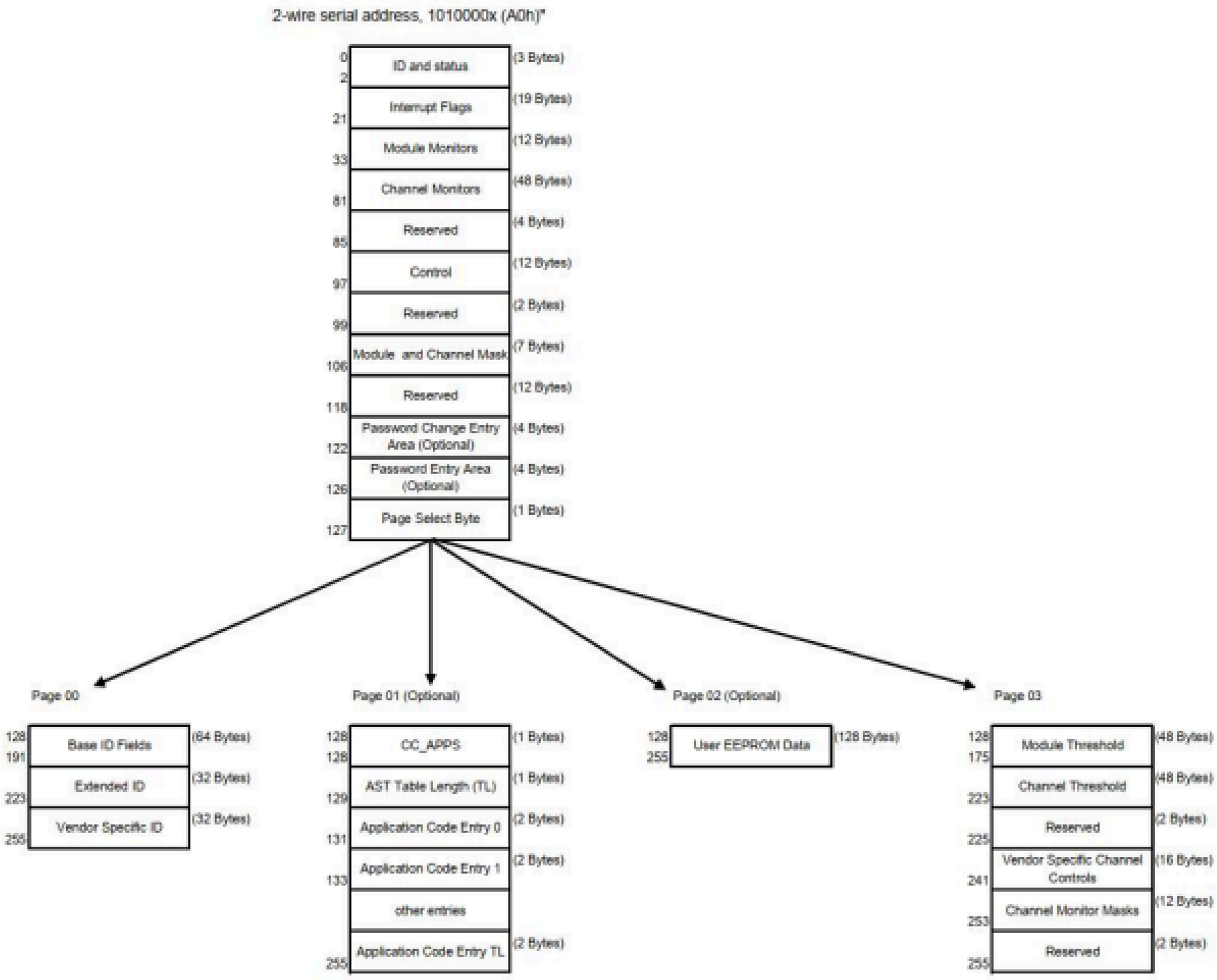
Receiver Optical Specification						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Notes**
Signal Speed Per Lane			10.3125± 100ppm		Gbps	
Lane Wavelength	L0	1295	1310	1325	nm	
	L1	1295	1310	1325	nm	
	L2	1295	1310	1325	nm	
	L3	1295	1310	1325	nm	
Damage threshold|Each Lane	THd	2.5			dBm	1
Average Receive Power|Each Lane		-12.6		2	dBm	
Receiver reflectance				-26	dB	
Sensitivity OMA|Each Lane[1]	Sen1			-12	dBm	2
Stressed Receiver Sensitivity (OMA), each Lane				-8.6	dBm	
LOS Assert	LOSA	-30	-		dBm	
LOS Deassert	LOSD			-17	dBm	
LOS Hysteresis	LOSH	0.5		5	dB	
Vertical Eye Closure Penalty	VECP	1.9			dB	3
Stressed Eye J2 Jitter	J2	0.3			UI	
Stressed Eye J4 Jitter	J4	0.47			UI	

Note:
1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
2. Measured with conformance test signal at receiver input for BER = 1e-12 .
3. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the recei

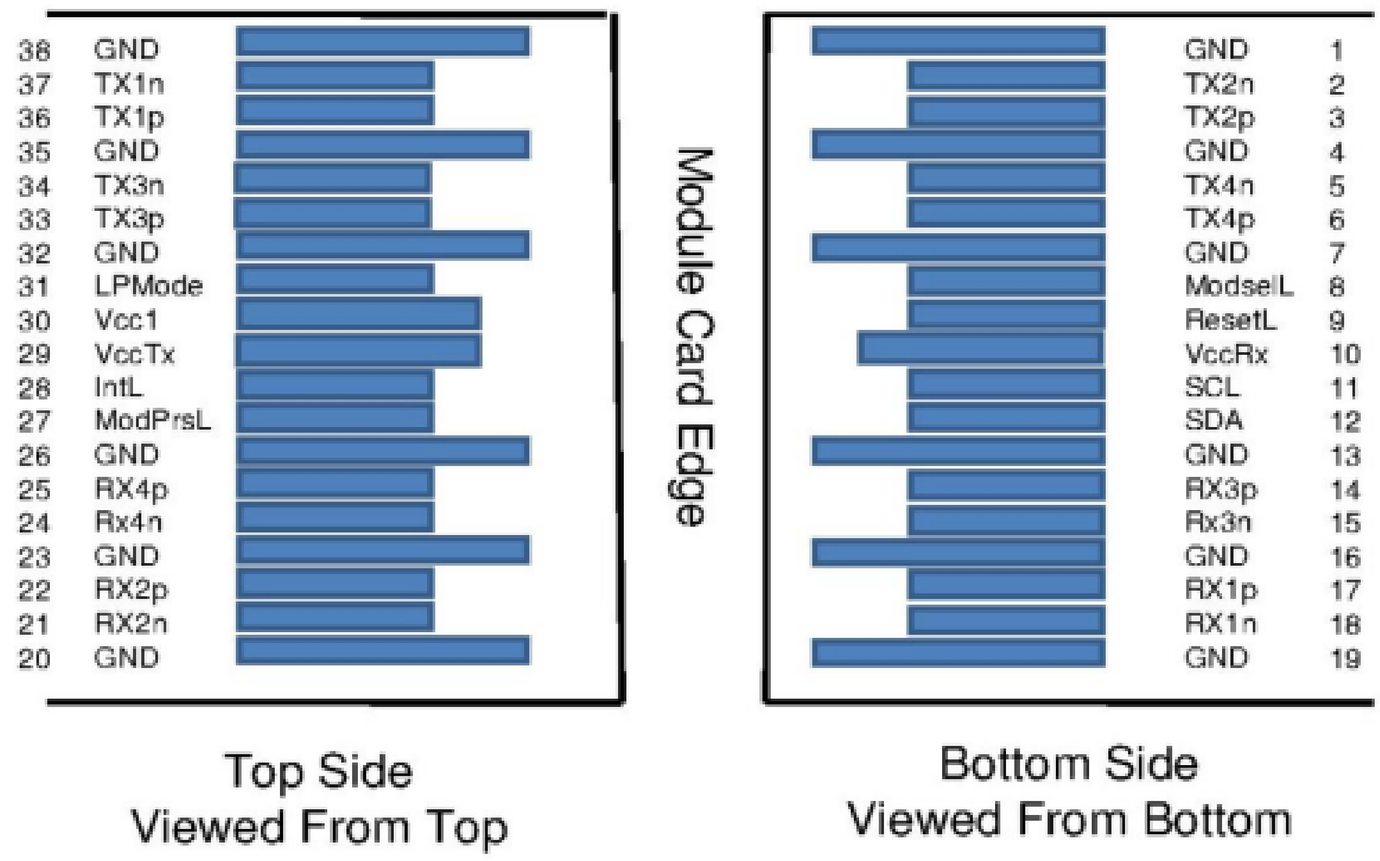
Digital diagnostic

Monitoring Interface				
Parameter	Symbol	Spec	Units	Condition/Notes
Temperature	Te	+/-3	°C	
Voltage	VCC	+/-5%	V	
IBias	BIAS	+/-10%	mA	
Rx power	Rx-pwr	+/-2	dBm	
Tx power	Tx-pwr	+/-2	dBm	

Memory Map



PIN DIAGRAM



Digital Diagnostics

PIN Description			
PIN	**Symbol**	**Name/Description**	**Note**
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3V Power Supply Receiver	2
11	SCL	2-Wire Serial Interface Clock	
12	SDA	2-Wire Serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3 V Power Supply transmitter	2
30	Vcc1	+3.3 V Power Supply	2
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data output	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data output	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1
Notes			

Notes 1:GND is the symbol for signal and supply (power) common for the QSFP module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed . Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA

ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node must be biased to the “High” state in the module.In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any QSFP modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are m

ResetL

The ResetL pin must be pulled to Vcc in the QSFP module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module inidicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset

ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low” when inserted and deasserted “High” when the module is physically absent from the host connector

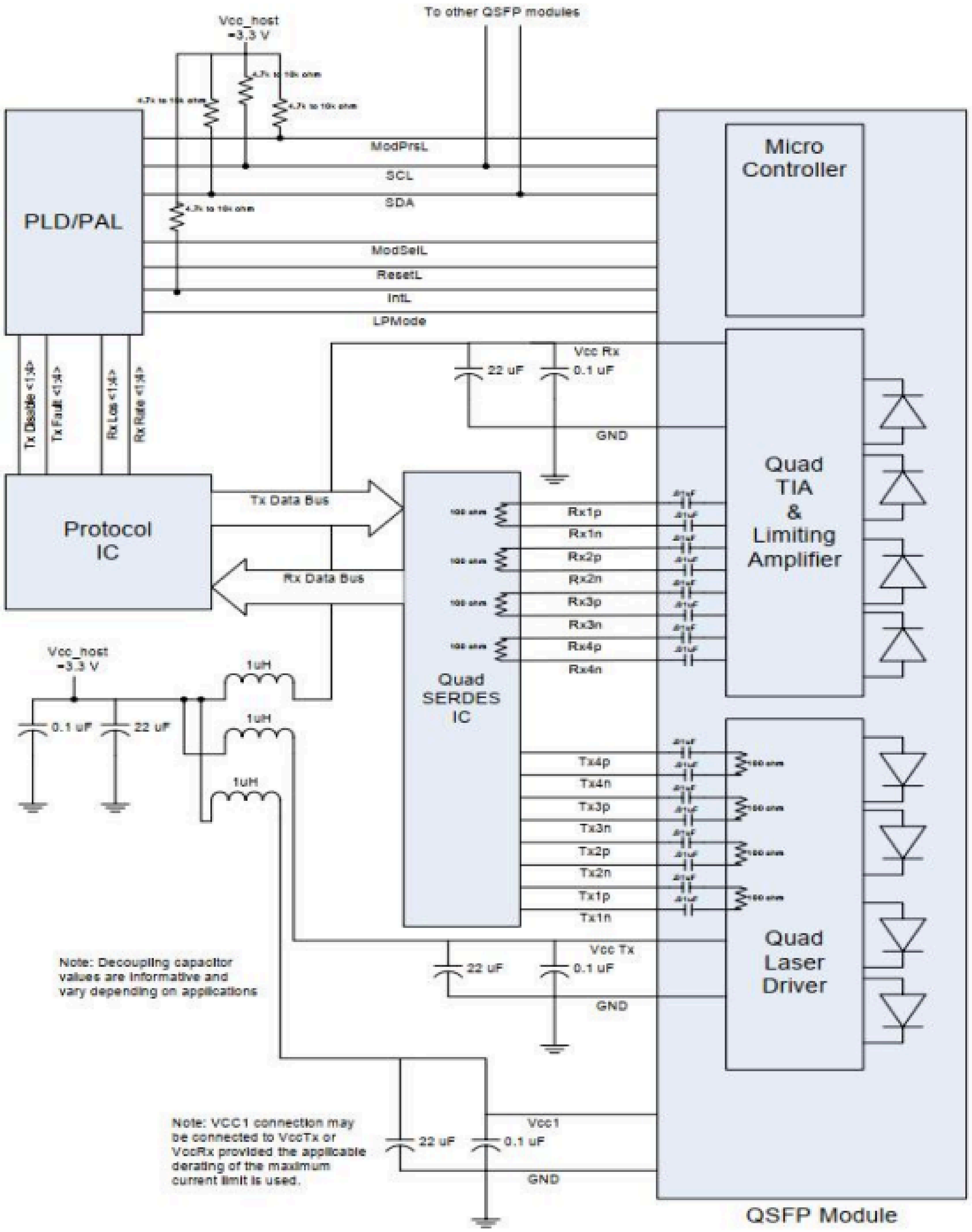
IntL

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface.The IntL pin is an open collector output and must be pulled to host supply voltage on the host boa

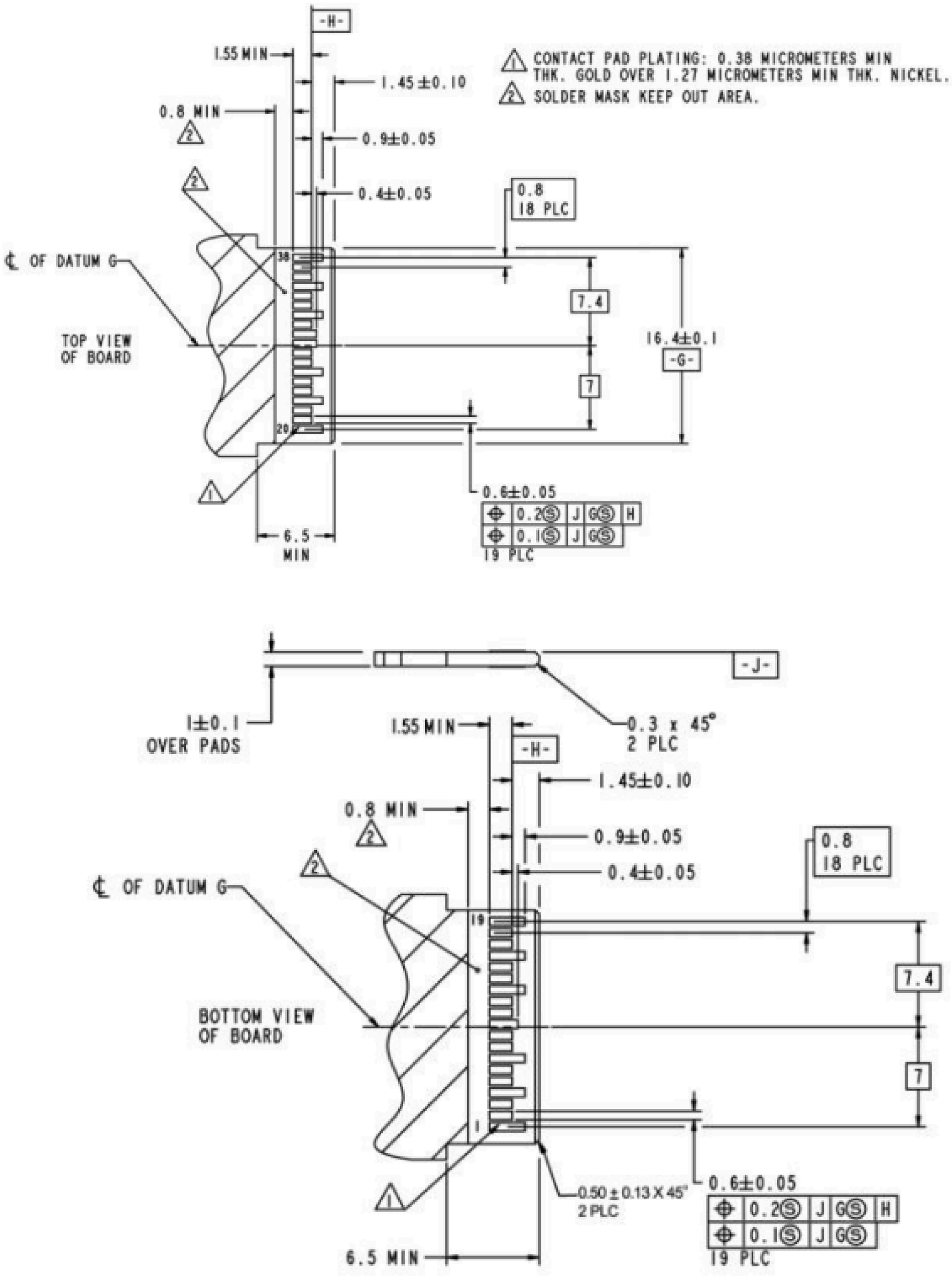
LPMode

The LPMode pin shall be pulled up to Vcc in the QSFP module. This function is affected by the LPMode pin and the combination of the Power_over-ride and Power_set software control bits (Address A0h, byte 93 bits 0,1). The module has two modes a low power mode and a high power mode. The high power mode operates in one of the four power classes. When the module is in a low power mode it has a maximum power consumption of 1.5W. This protects hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. The modules 2-wire serial interface and all laser safety functions must be fully operational in this low power mode. The module shall still support the completion of reset interrupt in this low power mode. If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate a power consumption greater than 1.5W and the module is in low power mode it must reduce its power consumption to less than 1.5W while still maintaining the functionality above. The exact method of accomplishing low power is not specified, however it is likely that either the Tx or Rx or both will not be operational in this state. If the Extended Identifier bits (Page 00h, byte 129 bits 6-7) indicate that its power consumption is less than 1.5W then the module shall be fully functional independent of whether it is in low power or high power mode. The Module should be in low power mode if the LPMode pin is in the high state, or if the Power_ over□ride bit is in the high state and the Power_set bit is also high. The module should be in high power mode if the LPMode pin is in the low state, or the Power_over-ride bit is high and the Power_set bit is low. Note that the default state for the Power_over-ride bit is low.

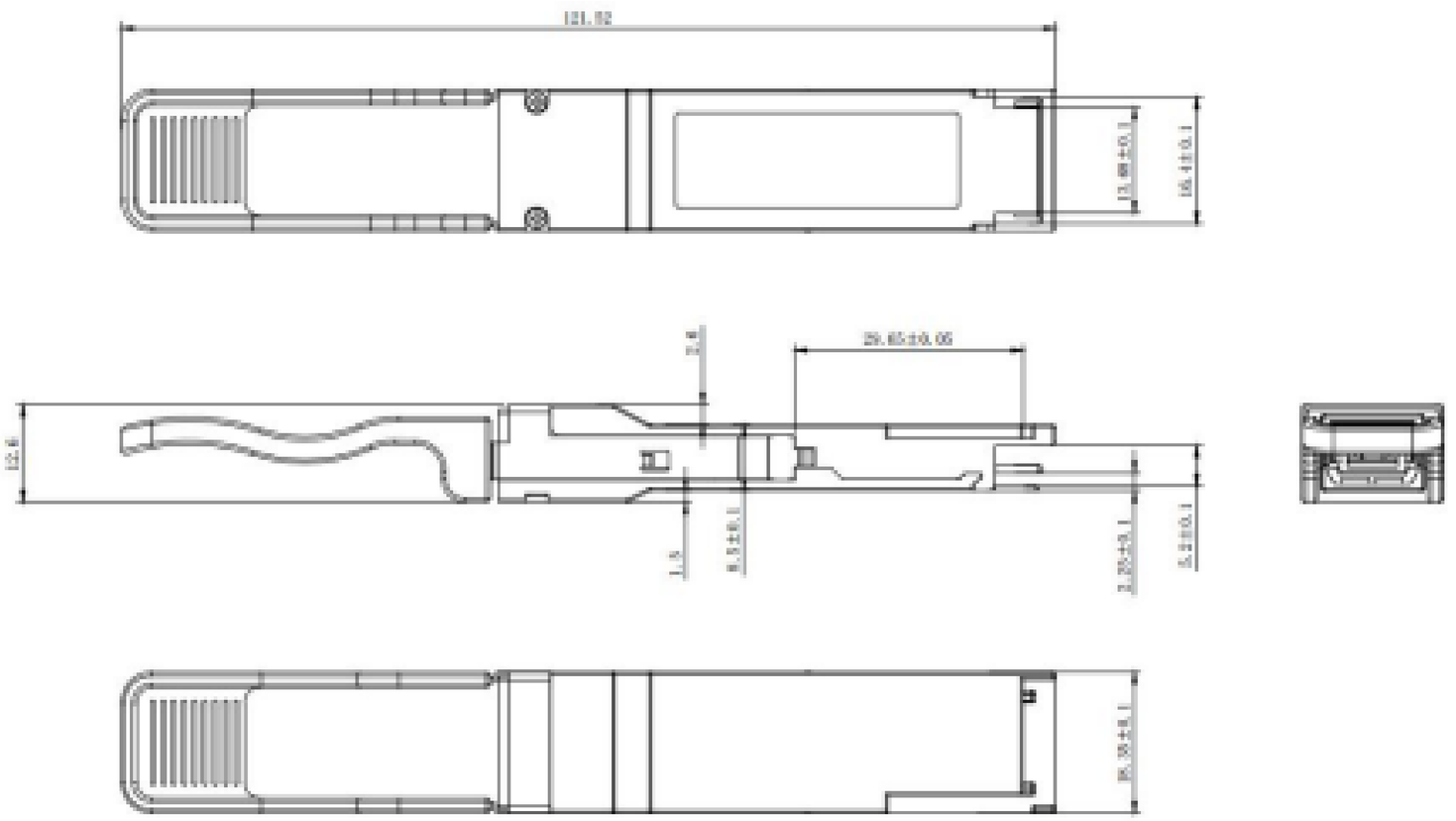
Electrical Interface

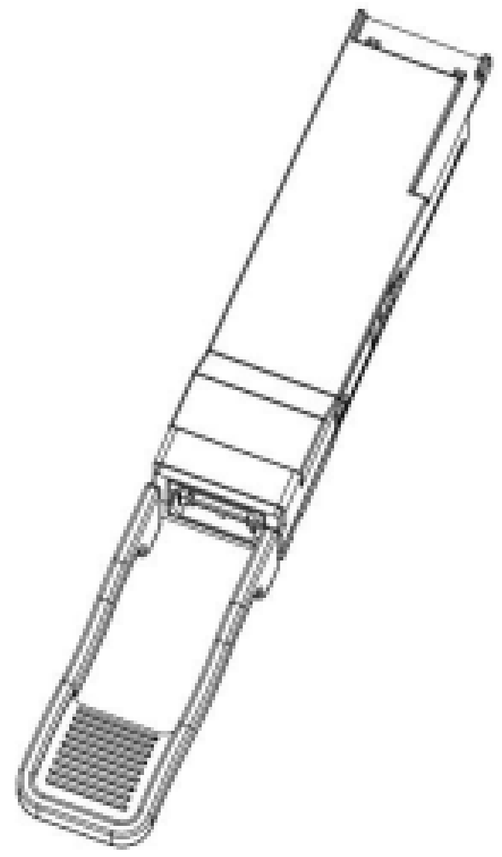


Recommended PCB Layout



Mechanical Dimensions





Notes:
1、Tolerance: +/-0.1mm.
2、Others according to SFF-8661 or customer spec .
3、Optical port according to fiber conn

Warnings

Handling Precautions:
This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety：
Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation